Inf2C, Computer Systems: Tutorial 3, Week 7

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1. **Ripple Carry Adder**
   Assume that the propagation delay in each gate in a 32-bit ripple carry adder is 100ps. How fast can a 32-bit addition be performed? Assuming that the adder delay is the major limiting factor on the clock speed, how fast can we clock the processor?

2. **Modulo-6 Counter**
   Design a synchronous Modulo-6 counter that will be able to count up to 5 clock positive edges. When it reaches 5, it resets to 0 and it starts the whole process again. In order to design this counter you can use D flip-flops and any two or three input gate you like.

3. **Datapath**
   Discuss the steps in executing the `jal`, the `lw` and the `add` instruction in the multiclock datapath presented in Figure 1.

   Now assume that an access to the register file takes 6.5ns, an access to the memory takes 100ns and the ALU delay is 6ns. Assume also that the instruction's execution stalls when it waits for a resource to produce a result. If we were to optimize this simple processor, which should be the component we should spend our main design efforts on, what could we do to improve it?

4. **Pipeline**
   What is the advantage of having a pipelined processor? Make sure you recall what structural and data hazards are. Consider a five stage MIPS pipeline. Assume that the processor has one memory port. Track the state of the pipeline at each cycle while executing the following sequence of instructions.

   ```
   add $t0, $t3, $t4
   lw $t2, 4($t4)
   add $t3, $t2, $t1
   lw $t8, 3($t9)
   add $t4, $t5, $t6
   xor $t1, $t2, $t3
   add $t7, $t3, $t4
   ```

   Will adding a memory port change anything?

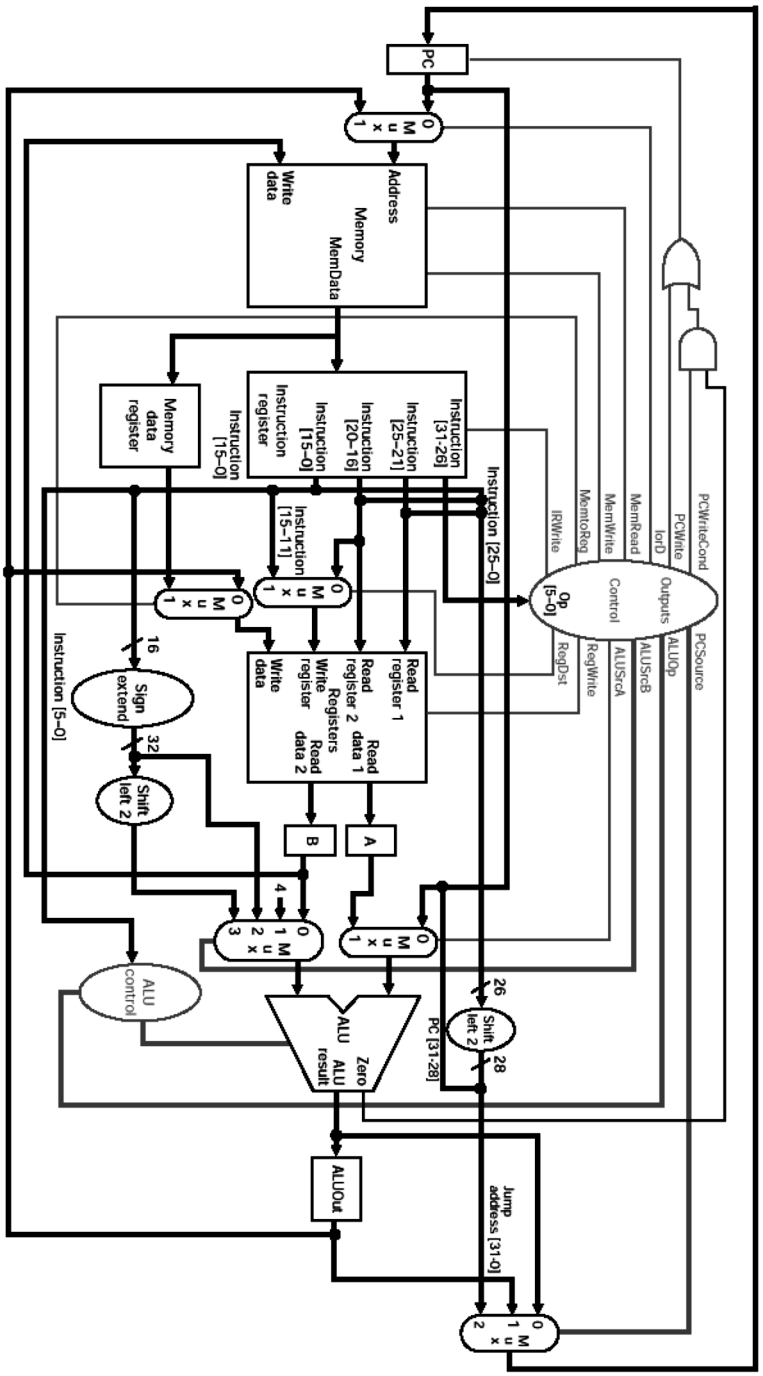

Figure 1: MIPS Datapath