Lecture 6: Hardware

Michael O’Boyle
Embedded Software
Overview

• Power and Energy
• Processors
  • Energy Efficiency
  • Code Size
• DSPs
  • Address generating Units
  • Specialised Arithmetic
• Multimedia Instructions
  • VLIW
• Reconfigurable
Power and Energy

- Energy and Power are first class issue in embedded and systems design
  - Battery life
  - Energy density, thermal
  - Environment - no more data centres in London

- Energy not always the same
  - A processor that is more power-hungry but takes less time may use less energy

\[ E = \int P(t) \, dt \]
"inherent power efficiency of silicon"
Processors

• Vast majority of embedded systems based on (semi-)programmable processors rather than specialised hardware (ASICs)
  • Ease of programming, upgrade or change of use
• Variety of ways to manage power

Example: STRONGARM SA1100

RUN: operational
IDLE: a SW routine may stop the CPU when not in use, while monitoring interrupts
SLEEP: Shutdown of on-chip activity
Dynamic Voltage Scaling

Power consumption of CMOS circuits (ignoring leakage):

\[ P = \alpha \cdot C_L \cdot V_{dd}^2 \cdot f \quad \text{with} \]
\[ \alpha : \text{switching activity} \]
\[ C_L : \text{load capacitance} \]
\[ V_{dd} : \text{supply voltage} \]
\[ f : \text{clock frequency} \]

Delay for CMOS

\[ \tau = k \cdot C_L \cdot \frac{V_{dd}}{(V_{dd} - V_t)^2} \quad \text{with} \]
\[ V_t : \text{threshold voltage} \]
\[ (V_t < \text{than } V_{dd}) \]

- Decreasing voltage slows down linearly, quadratic power saving
- Intel SpeedStep has 6 speed/voltage settings
- ARM has big.LITTLE offering
Multi-core: Reduce Power for same performance?

**Basic equations**

- **Power:** \( P \sim V_{DD}^2 \),
- **Maximum clock frequency:** \( f \sim V_{DD} \),
- **Energy to run a program:** \( E = P \times t \), with: \( t = \text{runtime (fixed)} \),
- **Time to run a program:** \( t \sim 1/f \),

**Changes due to parallel processing, with \( \beta \) operations per clock:**

- **Clock frequency reduced to:** \( f' = f / \beta \),
- **Voltage can be reduced to:** \( V_{DD}' = V_{DD} / \beta \),
- **Power for parallel processing:** \( P^\circ = P / \beta^2 \) per operation,
- **Power for \( \beta \) operations per clock:** \( P' = \beta \times P^\circ = P / \beta \),
- **Time to run a program is still:** \( t' = t \),
- **Energy required to run program:** \( E' = P' \times t = E / \beta \)

**Argument in favour of voltage scaling and parallel processing**
Code Size

- Memory costs. Reducing code size in ROM can be significant. CISC helps

- Reduction to 65-70% of original code size
- 130% of ARM performance with 8/16 bit memory
- 85% of ARM performance with 32-bit memory
Specialised Processors

- Filtering in digital signal processing. Signal at $t(s)$ depends on weighted avg of $k$ previous inputs.

\[ x_s = \sum_{k=0}^{n-1} w_{s-k} \cdot a_k \]

-- outer loop over
-- sampling times $t_s$

\{ MR:=0; A1:=1; A2:=s-1; \\
MX:=w[s]; MY:=a[0]; \\
for (k=0; k <= (n-1); k++) \\
{ MR:=MR + MX \cdot MY; \\
  MX:=w[A2]; MY:=a[A1]; \\
  A1++; A2--; \\
} \\
x[s]:=MR; \\
\}

Maps nicely but specialised

Wednesday, 30 January 2013
DSPs

- Specialised processors found in many embedded settings

- Have a number of special features
  - Specialised addressing modes
  - Separate addressing Unit
  - Saturating Arithmetic
  - Fixed Point Arithmetic
  - Real-time capabilities
  - Zero-overhead loops
  - Multiple memory banks
  - Heterogeneous register files
  - Multiply/accumulate instructions
Address generating Units

- Data memory can only be fetched with address contained in A,
- but this can be done in parallel with operation in main data path (takes effectively 0 time).
- A := A ± 1 also takes 0 time,
- same for A := A ± M;
- A := <immediate in instruction> requires extra instruction

Minimize load immediates
Specialised Arithmetic

- Returns largest/smallest number in case of over/underflows
- Example:
  a
  b
  +
____________________
standard wrap around arithmetic (1)0000
saturating arithmetic 1111
____________________
(a+b)/2: correct 1000
  wrap around arithmetic 0000
  saturating arithmetic + shifted 0111
  “almost correct”

- Appropriate for DSP/multimedia applications:
  - No timeliness of results if interrupts are generated for overflows
  - Precise values less important
  - Wrap around arithmetic would be worse.
Multimedia Instructions

- Multimedia instructions exploit that many registers, adders etc are quite wide (32/64 bit), whereas most multimedia data types are narrow
- 2-8 values can be stored per register and added. E.g.:

\[
\begin{align*}
\text{32 bits} & \quad \begin{array}{c}
\text{a1} \\
\text{a2}
\end{array} & \quad \begin{array}{c}
\text{b1} \\
\text{b2}
\end{array} \\
\text{+} & \\
\text{32 bits} & \quad \begin{array}{c}
\text{c1} \\
\text{c2}
\end{array}
\end{align*}
\]

- 2 additions per instruction; no carry at bit 16

- Cheap way of using parallelism
- SSE instruction set extensions, SIMD instructions
VLIW

- Instructions included in long instruction packets.
- Instruction packets are assumed to be executed in parallel.
- Fixed association of packet bits with functional units.

- Complexity of finding parallelism is moved from the hardware (RISC/CISC processors) to the compiler;
- Ideally, this avoids the overhead (silicon, energy, ..) of identifying parallelism at run-time.

A lot of expectations into VLIW machines

- However, possibly low code efficiency, due to many NOPs

Explicitly parallel instruction set computers (EPICs) are an extension of VLIW architectures: parallelism detected by compiler, but no need to encode parallelism in 1 word.
VLIW

- Instructions included in long instruction packets.
- Instruction packets are assumed to be executed in parallel.
- Fixed association of packet bits with functional units.
- Compiler is assumed to generate these “parallel” packets.
- Complexity of finding parallelism is moved from the hardware (RISC/CISC processors) to the compiler;
  - Ideally, this avoids the overhead (silicon, energy, ..) of identifying parallelism at run-time.

A lot of expectations into VLIW machines

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Explicitly parallel instruction set computers (EPICs) are an extension of VLIW architectures: parallelism detected by compiler, but no need to encode parallelism in 1 word.
Micro Controller: MHS 80C51

- 8-bit CPU optimised for control applications
- Extensive Boolean processing capabilities
- 64 k Program Memory address space
- 64 k Data Memory address space
- 4 k bytes of on chip Program Memory
- 128 bytes of on chip data RAM
- 32 bi-directional and individually addressable I/O lines
- Two 16-bit timers/counters
- Full duplex UART
- 6 sources/5-vector interrupt structure with 2 priority levels
- On chip clock oscillators
- Very popular CPU with many different variations
MPSoCs

TI OMAP5430 SoC

## MPSoCs

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Reconfigurable

• Custom HW may be too expensive, SW too slow.

Combine the speed of HW with the flexibility of SW
• HW with programmable functions and interconnect.
• Use of configurable hardware;
  common form: field programmable gate arrays (FPGAs)

Applications:
  § algorithms like de/encryption,
  § pattern matching in bioinformatics,
  § high speed event filtering (high energy physics),
  § high speed special purpose hardware.

Very popular devices from
  § XILINX, Actel, Altera and others
Memories typically used as look-up tables to implement any Boolean function of \( \leq 6 \) variables.

Processors typically implemented as “soft cores” (microblaze)
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