Computer Architecture - tutorial 2

Context, Objectives and Organization

The goal of the quantitative exercise in this tutorial, which covers Lecture 4 (pipelining and pipeline hazards), is to work through the scheduling of loops for the 5-stage MIPS pipeline. The exercise is extracted from the H&P book 3rd edition.

E1: groups of 2: 50 minutes

Problem

Use the following code fragment:

```
loop: LD     R1,0(R2)
      DADDI  R1,R1,1
      SD     0(R2),R1
      DADDI  R2,R2,4
      DSUB   R4,R3,R2
      BNEZ   R4,loop
```

Assume that the initial value of R3 is R2+396. Throughout this exercise use the classic RISC five-stage integer pipeline in H&P. Specifically, assume that: 1) branches are resolved in the second stage of the pipeline; 2) there are separate instruction and data memories; 3) all memory accesses take 1 clock cycle.

a. Show the timing of this instruction sequence for the RISC pipeline *without* any forwarding or bypassing hardware but assuming a register read and a write in the same clock cycle "forwards" through the register file. Assume that the branch is handled by flushing the pipeline. If all memory references take 1 cycle, how many cycles does this loop take to execute?
b. Show the timing of this instruction sequence for the RISC pipeline with normal forwarding and bypassing hardware. Assume that the branch is handled by predicting it as not taken. If all memory references take 1 cycle, how many cycles does this loop take to execute?
c. Assume the RISC pipeline with a single-cycle delayed branch and normal forwarding and bypassing hardware. Schedule the instructions in the loop including the branch delay slot. You may reorder instructions and modify the individual instructions operands, but do not undertake other loop transformations that change the number or opcode of the instructions in the loops. Show a pipeline timing diagram and compute the number of cycles needed to execute the entire loop.

You may use the following pipeline representation diagrams to develop your solution:

a.

Inst.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

b.

Inst.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

c.

Inst.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

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