

## What is Computer Architecture?



Metrics of interest for computer architects

- Performance
- Cost
- Reliability
- Power
- Area



- Metrics:
  - Execution time, response time: overall time for a given computation (e.g. full program execution, one transaction)
  - Latency: time to complete a given task (e.g. memory latency, I/O latency, instruction latency)
  - Bandwidth, throughput: rate of completion of tasks (e.g. memory bandwidth, transactions per second, MIPS, FLOPS)
- MHz, MIPS, FLOPS: must use with caution
- Benchmarking:
  - toy benchmarks, synthetic benchmarks, kernels, real programs,
  - Input sets
  - E.g. SPECint, SPECfp, EEMBC Coremark



A is n times faster than B means

Execution time of B

Execution time of A

#### A is m% faster than B means

Execution time of B – Execution time of A x100 = m

Execution time of A



- Take advantage of parallelism
  - System level: multiple processors, multiple disks
  - Processor level: pipelining, superscalar issue
  - Circuit level: carry-lookahead ALU
- Principle of locality
  - Spatial and Temporal Locality
  - 90% of program executing in 10% of code
  - E.g. Caches
- Focus on the common case
  - Amdahl's law, CPU Performance equation
  - E.g. RISC design principle



#### Speedup due to an enhancement E:



Suppose that enhancement E accelerates a fraction F of the task by a factor S, and the remainder of the task is unaffected, what is the *Execution time<sub>after</sub>* and *Speedup(E)*?



Execution time<sub>after</sub> = ExTime<sub>before</sub> × 
$$[(1-F) + \frac{F}{S}]$$





Q: Floating point instructions improved to run 2X; but only 10% of execution time are FP ops. What is the execution time and speedup after improvement?

Ans:

F = 0.1, S = 2  $ExTime_{after} = ExTime_{before} \times [(1-0.1) + 0.1/2] = 0.95 ExTime_{before}$   $Speedup = \frac{ExTime_{before}}{ExTime_{after}} = \frac{1}{0.95} = 1.053$ 

Instruction count (IC)

- Compiler, ISA

Cycles per instruction (CPI)

- ISA, microarchitecture

Clock time (1/f)

- Microarchitecture, technology

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## **CPU** time = **IC** x **CPI** x **Clock** time

**CPU time =** 
$$\left(\sum_{i=1}^{n} IC_{i} \times CPI_{i}\right) \times Clock time$$

where:  $IC_i = IC$  for instruction (instruction group) i  $CPI_i = CPI$  for instruction (instruction group) i

$$\mathbf{CPI} = \frac{\left(\sum_{i=1}^{n} \mathbf{IC}_{i} \times \mathbf{CPI}_{i}\right)}{\mathbf{IC}} = \sum_{i=1}^{n} \left(\mathbf{CPI}_{i} \times \frac{\mathbf{IC}_{i}}{\mathbf{IC}}\right)$$

# **Examples**



#### **Example:** • Branch instructions take 2 cycles, all other instructions take 1 cycle

- CPU A uses extra compare instruction per branch
- Clock frequency of CPU A is 1.25 times faster than CPU B
- On A 20% of instructions are branches (thus other 20% are compare instructions)

Find the CPU time

$$CPI_{A} = CPI_{branch} \times \frac{IC_{branch}}{IC} + CPI_{others} \times \frac{IC_{others}}{IC} = 2 \times 0.2 + 1 \times 0.8 = 1.2$$
$$CPI_{B} = CPI_{branch} \times \frac{IC_{branch}}{IC} + CPI_{others} \times \frac{IC_{others}}{IC} = 2 \times 0.25 + 1 \times 0.75 = 1.25$$

CPU time  $_{B} = IC_{B} \times CPI_{B} \times Clock time _{B} = 0.8 \times IC_{A} \times 1.25 \times (1.25 \times Clock time_{A})$  $= 1.25 \times IC_{A} \times Clock time _{A}$   $= IC_{A} \times Clock time _{A}$ 

**CPU A is faster!** 

Inf3 Computer Architecture - 2015-2016



IC:

- Compiler optimizations (constant folding, constant propagation)
- ISA (More complex instructions)

CPI:

- Microarchitecture (Pipelining, Out-of-order execution, branch prediction)
- Compiler (Instruction scheduling)
- ISA (Simpler instructions)

Clock period:

- Hardware (Smaller transistors Moore's law)
- ISA (Simple instructions that can be easily decoded)
- Microarchitecture (Simple architecture)