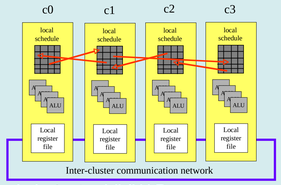
ICSA Industrial Research Collaborations

Recent history of research work interacting with microprocessor IP companies

Early Clustered VLIW Research

This project ran from 1996-99, in collaboration with UPC Barcelona, developing scalable VLIW architectures and compiler techniques. This led to the concept of Clustered VLIW, in which clusters of functional units share resources and may also share values with neighbouring clusters. The Distributed Modulo Scheduling algorithm was developed to produce highly-efficient code schedules for compute-bound loop nests.



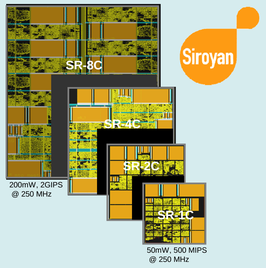
A 4-cluster VLIW Processor

1. M. Fernandes, N.P. Topham and J. Llosa, **Distributed Modulo Scheduling**, in *Proc. 5th Annual International IEEE Conf. on High Perf. Comp. Architecture* (HPCA-5), Orlando Fl, 1998.

The Siroyan OneDSP Processor

In 1999 Topham co-founded Siroyan, a UK intellectual property startup company, with the aim of developing a scalable DSP based on the clustered VLIW concept. The architecture was announced at Microprocessor Forum in 2001, and shortly afterwards a 2-cluster implementation was produced in 0.18um and 0.15um silicon. The company filed 13 worldwide patents on innovationd in architecture, microarchitecture and compiler algorithms.

In 2003 the Siroyan OneDSP design and its associated intellectual property was acquired by the Altera Corporation Inc, the second largest manufacturer of FPGA devices.



Die plots showing four versions of OneDSP

2. N.P. Topham, **The Siroyan OneDSP Architecture**, *Microprocessor Forum,* San Jose 2001.

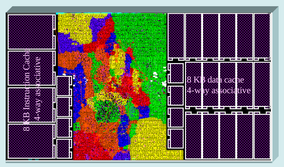
Architecting the ARC 600 Configurable Processor

In 2003 Topham led a team within ARC International (LSE:ARK) to develop an ultra low-power configurable processor, based around the ARCompact instruction set. This was announced at Microprocessor Forum in 2003.

Shortly after completing the ARC 600, Topham returned to The University of Edinburgh to take up the Chair in Computer Systems. This began a collaboration between ARC and the University which continues to the present day. The ARC 600 has been widely licensed and deployed in areas ranging from USB flash storage to mobile TV.

Selection of publicly-announced ARC 600 licensees since 2003

290 MHz worst-case **0.13um** ASIC process
Dimensions: 1.05mm x 1.87mm (**2 sq.mm**)



Die plot showing ARC 600 floorplan [3]

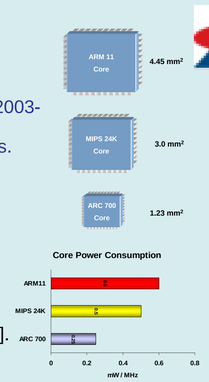
3. N.P. Topham, **The ARC 600 Architecture**, *Microprocessor Forum,* SanJose 2003.

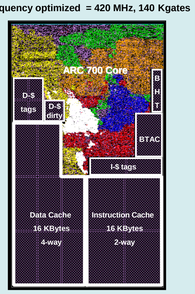
The ARC 700 Configurable Processor

There has been a continuous collaboration between ARC and ICSA to optimize the performance of the ARC 700, a high-performance configurable core developed during 2003-04. The ARC 700 has also been widely licensed and deployed in areas ranging from network processors, media processors, mobile handsets, and communications satellites.

Selection of publicly-announced ARC 700 licensees since 2004

Die area and power consumption comparisons with simliar ARM and MIPS cores [4].





4. N.P. Topham, **Secrets of the ARC 700 Revealed**, *Embedded Processor Forum,* 2004.

The ARC Video Processor

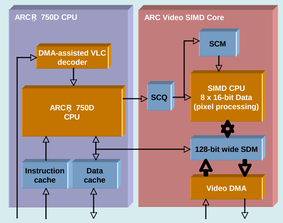
In 2005, ARC and ICSA collaborated on the architecture of a high performance, low power, configurable media processor targeting mobile video applications. The ARC Video and ARC Sound Advanced products are now in production and licensed to a number of fabless semiconductor companies developing portable media devices.

A number of innovative architectural concepts are combined in ARC Video to sustain high performance at very low power consumption.

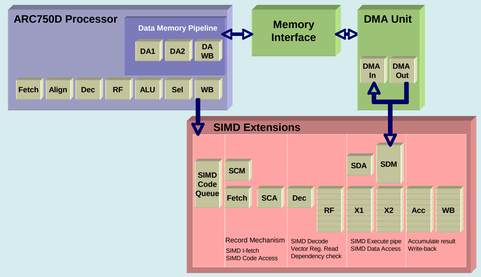
For example, it is able to decode standard TV resolution H.264, VC-1, MPEG-2 or MPEG-4 video streams (2 Mbps, 30 fps) when running at only 166 MHz. At that frequency, a design implemented in 90nm silicon processes will consume as little as 45 mW.

MPEG-2 and MPEG-4 decoders for the ARC Video architecture were developed in the School of Informatics, in collaboration with ARC.

The resulting MPEG-2 decoder can decode a standard definition video (30 fps) on an ARC Video processor running at just 100 MHz and consuming only 25 mW. This is believed to be the lowest-power software solution for MPEG-2 decoding available today.

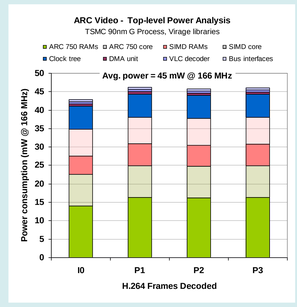


Block diagram of ARC Video architecture

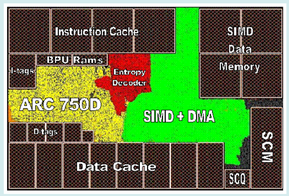


Pipeline structure of the ARC SIMD core

Publicly-announced ARC Video licensees



Power analysis of ARC Video [6]



Die plot of ARC Video core [5]

- **3.25 mm² in a 90nm TSMC G process**
- **H.264 D1 30fps at 160 MHz**
- **40 mW power consumption**

5. N.P. Topham, **ARC's SIMD Extensions for Multimedia Applications**, *Fall Processor Forum,* San Jose and Tokyo 2005.
6. N.P. Topham, **Low Power Challenges in High Performance Media Processors**, Fall Processor Forum, (invited seminar) San Jose 2006.

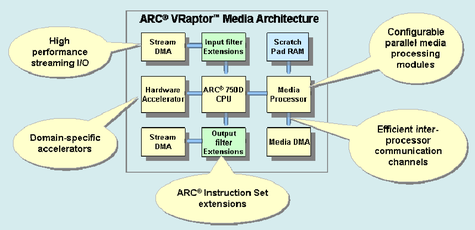
Scalable Multi-core Media Processing

During 2006, ARC and ICSA have been collaborating on the design of a scalable multi-core media processor architecture. This was announced in October 2006 and will form the basis of a range of platforms for very high performance media processing.

Each CPU can control up to 8 independent Media Processors.

A new and novel interconnection protocol supports event-driven processing directly in hardware, and achieves extremely low latency communication – as seen by software.

Products based on this architecture will be announced in 2007.



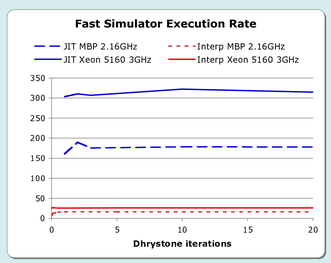
7. N.P. Topham, **Introducing the ARC® VRaptor™ Media Architecture**, *Fall Processor Forum,* San Jose and Tokyo 2006.

JIT-translation for High Speed CPU Simulation

The ICSA micro-architecture research team have developed one of the worlds fastest CPU functional simulators. This uses a patent-pending[1] dynamic JIT translation mechanism to achieve simulation speeds up to **322 million** instructions per second on a 3 GHz host[2].

For typical embedded RISC processors, with CPI of 1.3, this represents an effective simulated clock rate of over 400 MHz.

This technology could be deployed commercially, across a wide range of different embedded CPU architectures. Licensing discussions are currently in progress.



2. Measured on a Dell PE1950, Intel Xeon 5160 CPU 2.99GHz, 4 MB L2 cache, 4GB memory.

1. N. Topham, UK Patent application no. 0621711.1, filed 1st November 2006.

School of informatics